IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

Please amend the claims as follows:

1. (amended) A method of fabricating a semiconductor device to be assembled in a facedown orientation on a test substrate, comprising:

providing at least one of a semiconductor device having contact pads and a test substrate having test pads; and

disposing at least one stabilizer on a surface of at least one of said semiconductor device and said test substrate in a location sufficient to at least partially stabilize an orientation of said semiconductor device upon assembly with said test substrate.

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2. The method of claim 1, wherein said disposing said at least one stabilizer comprises disposing a plurality of stabilizers on said surface.

3. The method of claim 2, wherein said disposing said plurality of stabilizers comprises disposing at least one stabilizer of said plurality of stabilizers adjacent at least one corner of said surface.

4. (amended) The method of claim 2, wherein said disposing said plurality of stabilizers comprises disposing a first stabilizer of said plurality of stabilizers adjacent a first edge of said surface and disposing a second stabilizer of said plurality of stabilizers adjacent a second, opposite edge of said surface.

5. The method of claim 2, wherein said disposing said plurality of stabilizers comprises disposing a plurality of stabilizers on said surface to protrude a substantially uniform distance from said surface.

6. The method of claim 1, wherein said disposing said at least one stabilizer comprises fabricating said at least one stabilizer on said surface.

7. The method of claim 6, wherein said fabricating comprises fabricating said at least one stabilizer from a photopolymer.

8. The method of claim 7, wherein said fabricating comprises fabricating at least two superimposed, contiguous, mutually adhered layers.

9. The method of claim 1, wherein said providing comprises providing at least one semiconductor die.

10. The method of claim 1, wherein said providing comprises providing a semiconductor wafer with a plurality of semiconductor dice.

11. The method of claim 1, wherein said providing comprises providing a chip-scale package.

12. (amended) The method of claim 1, wherein said providing comprises providing both said semiconductor device and said test substrate and wherein said disposing comprises disposing at least one stabilizer on a surface of each of said semiconductor device and said test substrate.

13. (amended) The method of claim 1, wherein said disposing comprises adhering at least one preformed stabilizer to said surface.

14. The method of claim 1, further comprising, prior to said disposing, fabricating said at least one stabilizer from a photopolymer material.

15. The method of claim 14, wherein said fabricating comprises fabricating at least two superimposed, contiguous, mutually adhered layers.

16. The method of claim 1, wherein said disposing said at least one stabilizer comprises applying a layer of insulative material on said surface and selectively patterning said layer.

17. The method of claim 1, wherein said disposing said at least one stabilizer comprises applying a layer of photoresist material on said surface and selectively patterning said layer.

18. The method of claim 1, further comprising disposing at least one conductive structure in contact with at least one of said contact pads of said semiconductor device and said test pads of said test substrate.

19. The method of claim 18, wherein said disposing at least one conductive structure comprises forming at least one solder bump on at least one of said contact pads of said semiconductor device and said test pads of said test substrate.

20. (amended) The method of claim 18, wherein said disposing at least one conductive structure comprises applying at least one structure comprising a solder, a metal, a metal alloy, a conductor-filled epoxy, a conductive epoxy, or a z-axis conductive elastomer to at least one of said contact pads of said semiconductor device and said test pads of said test substrate.

21. The method of claim 18, further comprising selecting said at least one stabilizer to protrude from said surface at most a distance that said at least one conductive structure protrudes from said surface.

22. (amended) A method of fabricating a semiconductor device component, comprising:

providing at least one of a semiconductor device with contact pads exposed at a surface thereof and a test substrate with test pads exposed at a surface thereof; and

sequentially forming layers of at least one stabilizer on a surface of said at least one of said semiconductor device and said test substrate, said at least one stabilizer protruding from said surface and having a plurality of superimposed, contiguous, mutually adhered layers, each of said layers comprising a photopolymer, said at least one stabilizer being located on said surface so as to at least partially stabilize an orientation of said semiconductor device upon disposal thereof face-down on said test substrate.

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23. (amended) A method of fabricating a semiconductor device component, comprising:

placing at least one of a semiconductor device with contact pads and a test substrate with test pads in a horizontal plane;

recognizing a location and orientation of said at least one of said semiconductor device and said test substrate;

stereolithographically fabricating at least one stabilizer comprising at least one layer of semisolid material on a surface of said at least one of said semiconductor device and said test substrate, said at least one stabilizer being configured to at least partially stabilize an orientation of said semiconductor device upon disposal thereof face-down on said test substrate.

24. (amended) The method of claim 23, further comprising storing data including at least one physical parameter of said at least one of said semiconductor device and said test substrate and of said at least one stabilizer in computer memory, and using said stored data in conjunction with a machine vision system to recognize said location and orientation of said at least one of said semiconductor device and said test substrate.

25. The method of claim 24, further including in computer memory at least one parameter of another semiconductor device component with which each said at least one of said semiconductor device and said test substrate is to be assembled.

26. (amended) The method of claim 24, further comprising using said stored data, in conjunction with said machine vision system, to selectively apply said at least one layer of semisolid material stereolithographically to at least one portion of said surface.

27. (amended) The method of claim 24, further including securing at least one of said at least one substrate and said test substrate to a carrier prior to placing at least one of said at least one substrate and said test substrate in said horizontal plane.

28. The method of claim 24, further comprising recognizing a location of at least one of said contact pads of said semiconductor device and said test pads of said test substrate.

29. (amended) A method of assembling a semiconductor device with a test substrate, comprising:

providing a semiconductor device having contact pads exposed at a surface thereof;

selecting a test substrate having test pads on a surface thereof, said test pads being located correspondingly to at least selected ones of said contact pads;

securing at least one stabilizer to a surface of at least one of said semiconductor device and said test substrate; and

disposing said semiconductor device facedown on said test substrate with said at least selected ones of said contact pads in communication with corresponding ones of said test pads.

30. The method of claim 29, further comprising disposing conductive structures between said at least selected ones of said contact pads and said corresponding ones of said test pads.

31. The method of claim 29, wherein said securing comprises securing said at least one stabilizer to a surface of at least one of said semiconductor device and said test substrate to face another surface of the other of said semiconductor device and said test substrate upon said disposing.

32. The method of claim 29, wherein said securing comprises securing at least one stabilizer to each of said semiconductor device and said test substrate.

33. (amended) The method of claim 29, wherein said securing comprises securing at least one prefabricated stabilizer to said surface of said at least one of said semiconductor device and said test substrate.

34. (amended) The method of claim 33, further comprising stereolithographically fabricating said at least one prefabricated stabilizer.

35. (amended) The method of claim 33, wherein said securing comprises adhering said at least one prefabricated stabilizer to said surface of said at least one of said semiconductor device and said test substrate.

36. (amended) The method of claim 29, wherein said securing comprises fabricating said at least one stabilizer on said surface of said at least one of said semiconductor device and said test substrate.

37. (amended) The method of claim 29, further comprising positioning said at least one stabilizer on said surface of said at least one of said semiconductor device and said test substrate so as to at least partially stabilize said semiconductor device upon said disposing.

38. (amended) A semiconductor device, comprising:

a substrate having contact pads exposed at a surface thereof, said contact pads being configured to communicate with corresponding test pads of a test substrate upon disposing said substrate facedown over said test substrate; and

at least one stabilizer protruding from said surface, said at least one stabilizer being configured to at least partially stabilize an orientation of the semiconductor device upon disposal thereof facedown over said test substrate.

39. (amended) The semiconductor device of claim 38, wherein said at least one stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said test substrate upon disposing said substrate facedown over said test substrate.

40. (amended) The semiconductor device of claim 39, wherein said at least one stabilizer protrudes from said surface at most the distance between said plane of said surface of said substrate and said plane of said surface of said test substrate when at least one conductor connects at least one of said contact pads and a corresponding one of said test pads.

41. The semiconductor device of claim 38, wherein said at least one stabilizer comprises a dielectric material.

42. (amended) The semiconductor device of claim 38, wherein said at least one stabilizer comprises a photopolymer.

43. The semiconductor device of claim 42, wherein said photopolymer is at least semisolid.

44. The semiconductor device of claim 42, wherein said at least one stabilizer has a plurality of superimposed, contiguous, mutually adhered layers.

45. The semiconductor device of claim 38, wherein said at least one stabilizer is positioned to be located proximate a corner of said surface.

46. The semiconductor device of claim 38, wherein said at least one stabilizer is positioned to be located proximate an edge of said surface.

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47. The semiconductor device of claim 38, wherein said at least one stabilizer has a cross-sectional plan of one of quadrilateral, round, oval, and triangular.

48. The semiconductor device of claim 38, wherein said at least one stabilizer is elongated.

49. The semiconductor device of claim 38, wherein said substrate comprises a semiconductor wafer.

50. The semiconductor device of claim 38, wherein said substrate comprises a semiconductor die.

51. The semiconductor device of claim 38, wherein said substrate comprises a chip-scale package.

52. (amended) The semiconductor device of claim 38, wherein said test substrate also includes at least one stabilizer configured to at least partially stabilize said substrate upon disposing said substrate facedown over said test substrate.

53. (amended) A test substrate, comprising:

a substrate having test pads exposed at a surface thereof, said test pads being configured to communicate with corresponding contact pads of a semiconductor device to be disposed facedown over said substrate; and

at least one stabilizer protruding from said surface, said at least one stabilizer being configured to at least partially stabilize the semiconductor device upon disposal thereof facedown over a test substrate.

54. (amended) The test substrate of claim 53, wherein said at least one stabilizer protrudes from said surface at most a distance between a plane of said surface of said substrate and a plane of a surface of said semiconductor device upon disposing said semiconductor device facedown over said substrate.

55. (amended) The test substrate of claim 54, wherein said at least one stabilizer protrudes from said surface at most the distance between said plane of said surface of said substrate and said plane of said surface of said semiconductor device when at least one conductor connects at least one of said contact pads and a corresponding one of said test pads.

56. The test substrate of claim 53, wherein said at least one stabilizer comprises a photopolymer.

57. The test substrate of claim 56, wherein said photopolymer is at least semisolid.

58. The test substrate of claim 56, wherein said at least one stabilizer comprises a plurality of superimposed, contiguous, mutually adhered layers.

59. The test substrate of claim 53, wherein said semiconductor device has at least one stabilizer secured to a surface thereof, said at least one stabilizer configured to at least partially stabilize said semiconductor device upon disposal of said semiconductor device face-down over said substrate.

60. An assembly of a semiconductor device and a test substrate, comprising:
a test substrate with at least one test pad exposed at a surface thereof;

a semiconductor device with at least one contact pad exposed at a surface thereof, said surface of said semiconductor device facing said surface of said test substrate with said at least one contact pad in communication with said at least one test pad; and

at least one stabilizer disposed between said test substrate and said semiconductor device.

61. The assembly of claim 60, wherein said at least one stabilizer is secured to said surface of said test substrate.

62. The assembly of claim 60, wherein said at least one stabilizer is secured to said surface of said semiconductor device.

63. The assembly of claim 60, comprising a plurality of stabilizers, at least one of said plurality of stabilizers being secured to said surface of said test substrate and at least one other of said plurality of stabilizers being secured to said surface of said semiconductor device.

64. The assembly of claim 60, wherein said at least one stabilizer comprises a photopolymer.

65. The assembly of claim 60, wherein said photopolymer is at least semisolid.

66. The assembly of claim 64, wherein said at least one stabilizer has a plurality of superimposed, contiguous, mutually adhered layers.

67. The assembly of claim 60, wherein said at least one stabilizer extends between a plane of said surface of said test substrate and a plane of said surface of said semiconductor device at most a distance between said planes of said surfaces upon establishing communication between said at least one test pad and said at least one contact pad.

68. The assembly of claim 60, further comprising at least one conductive structure disposed between said test substrate and said semiconductor device.

69. (amended) The assembly of claim 68, wherein said at least one stabilizer extends between a plane of said surface of said test substrate and a plane of said surface of said semiconductor device at most a distance said at least one conductive structure extends between said planes of said surfaces.

70. (amended) A method for stabilizing a semiconductor device disposed facedown over a test substrate, comprising:

securing at least one stabilizer configured to at least partially stabilize the semiconductor device to a surface of at least one of the semiconductor device and the test substrate; and

inverting and positioning the semiconductor device over the test substrate so as to establish communication between at least one contact pad of the semiconductor device and a corresponding test pad of the test substrate.

71. The method of claim 70, wherein said securing comprises stereolithographically fabricating said at least one stabilizer on said surface.

72. (amended) The method of claim 70, wherein said securing comprises:

forming a first layer of material in an unconsolidated state over at least a portion of said surface; and

selectively altering a state of said first layer in a location to which said at least one stabilizer is to be secured to at least a partially consolidated state to form a first layer of said at least one stabilizer while leaving material in other portions of said first layer in said unconsolidated state.

73. The method of claim 72, further comprising repeating said forming and said selectively altering to fabricate a second layer of said at least one stabilizer.

74. The method of claim 70, further comprising disposing at least one conductive structure in contact with said at least one contact pad and said corresponding test pad.

IN THE DRAWINGS:

Accompanying this Preliminary Amendment is a Letter to the Chief Draftsman submitting proposed revisions to FIGS. 1, 2, 3, 6, 9, 12, 13, 17, 18. Approval of the revised figures is respectfully requested.